Constant Current Regulated Buck Controller with Active Power Factor Correction

Features

- High Voltage JFET Technology is Applied for Direct Power Supply of IC with No MLCC Buffer
- Capacitance Amplifier Technology is Applied for Loop Compensation with No MLCC Compensation
- Real Time Compensating Technology for High Precision (±3%) LED Current Control, Excellent Line and Load Regulation
- Soft Driving and Critical Conduction Mode Operation for Low EMI Optimization with Both Conduction and Radiation
- Constant On Time Control for Active PFC for High Power Factor (>0.95) and Low THD (<15%)
- Build-in 800V JFET and Integrated 650V MOSFET for 440 Vac Operation and 4kV Surge Capability
- Programmable Current Dropping At Both Low Line (e.g. <180 Vac) and High Line (e.g. > 350Vac) for Thermal and Reliability Performance
- Selected Output OVP for Kinds of Applications
- Maximum Switching Frequency Clamping for System Reliability and High Efficiency
- SOP7 Package

Protection

- Built-In Soft Start
- Thermal Regulation
- LED Open and Short Protection
- Cycle by Cycle Current Limit
- Leading Edge Blanking for Current Sensing
- Leading Edge Blanking for Zero Crossing Detection
- VCC Under Voltage Lock Out (UVLO) and Clamping

Application

- Non-isolated APFC BUCK LED Driver

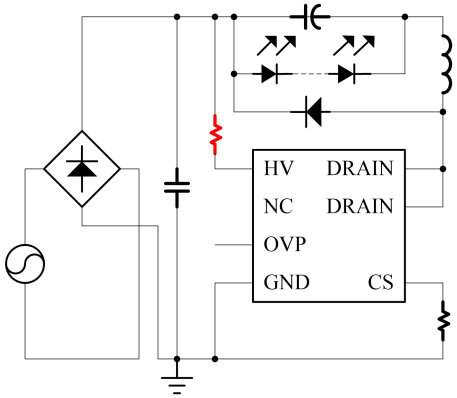


Fig. 1. Typical application circuit

- Recommended Operation Conditions With India Line Voltage (90-440Vac)

Input Power	Output Spec.	Part No.
20W Batten	*90V200*mA	YT2302DHS7
22W Batten	*90V220*mA	YT2302EHS7
20W Panel	*75V240*mA	YT2302EHS7
26W Batten	*90V260*mA	YT2302FHS7
24W Panel	*75V280*mA	YT2302EHS7

Address: Room 1501, Block A3, West Jianzhu Rd. 777, Binhu District, Wuxi, Jiangsu , China
Phone/Fax: 86-510-85388846

Package and Ordering Information

Part No.	Material Type	Package	Operating Temperature	Built-in MOSFET SPEC	Packing Method
YT2302DHS7	Green	SOP7	-40℃ to 105℃	700V4.5ohm	Tape 4000 pcs/Reel
YT2302EHS7	Green	SOP7	-40℃ to 105℃	650V3.7ohm	Tape 4000 pcs/Reel
YT2302FHS7	Green	SOP7	-40℃ to 105℃	650V2.7ohm	Tape 4000 pcs/Reel

Pin Configuration

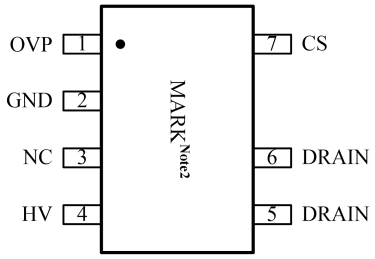


Fig. 2. Pin configuration for SOP7

Note 2： Please refer to the "Marking Rule".

Pin Definition

Pin No.	Name	Description
1	OVP	Over Voltage Protection.
2	GND	Ground.
3	NC	No Connection.
4	HV	High Voltage Input to The Internal JFET for Power Supply and Line Detection. A 15kohm Resistor Should be Connected from This Point to The Rectified Bus Line to Withstand the Surge.
5、6	DRAIN	Internal HV MOSFET Drain.
7	CS	Current Sense. Connect A Resistor to GND to Sense the Inductor Current.

Internal Block Diagram

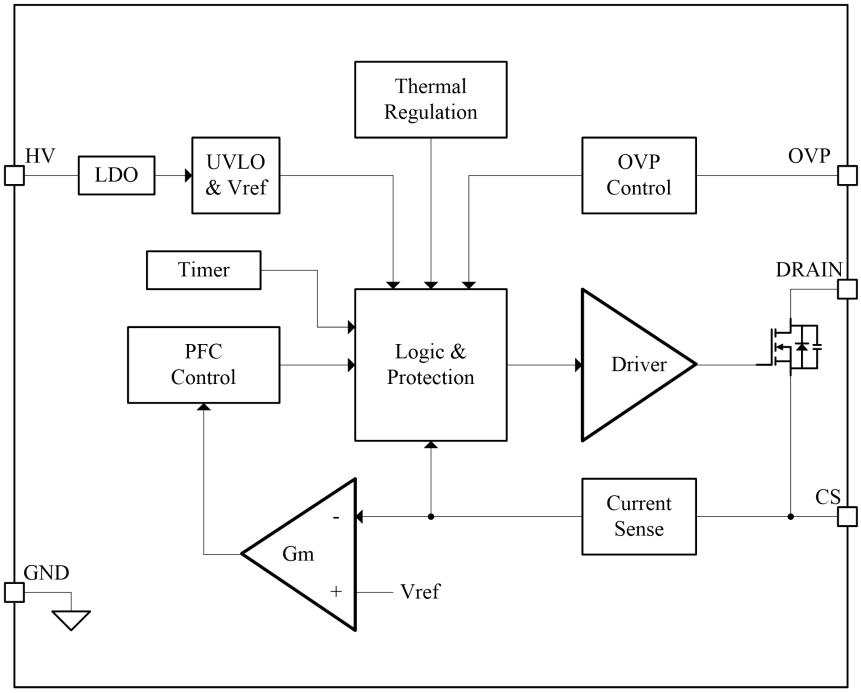


Fig. 3 Internal block diagram

Absolute Maximum Ratings[Note3]

Parameters	Symbol	Range	Units
"HV" voltage range	V_{HV}	-0.3 ~ 800	V
"CS" and "OVP" voltage range	V_{CS}, V_{OVP}	-0.3 ~ 6	V
Guaranteed minimum "DRAIN" voltage[Note4]	V_{DS_min}	650	V
ESD Human mode[Note5]	ESD_{hbm}	3000	V
Operating junction temperature range	T_j	-40 ~ 150	℃
Ambient temperature range	T_a	-40 ~ 105	℃
Storage Temperature Range	T_{stg}	-40 ~ 150	℃
Welding temperature (< 20 *s* welding)	T_{lead}	260	℃
Junction to ambient thermal resistance	θ_{thja}	145	℃/W

Note3：Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Note4：Depending on the different built-in MOSFET SPEC, see the corresponding relationship between the model and the built-in MOSFET.

Note5： Electrical components and circuit boards will be aware of the situation in the discharge is not easy. Although this product has a special electrostatic protection circuit, but in the case of high-energy electrostatic discharge, the chip may have damage and loss of function or performance degradation. Therefore, users still need to take appropriate preventive measures ESD.

Electrical Characteristics[Note6] (Unless otherwise specified, T_a = 25 ℃)

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
VCC						
VCC Turn On Threshold	V_{CC_ON}	V_{CC} Rising			10	V
VCC Operating Current	I_{CC_OP}			200	360	μA
PWM						
Minimum On Time	T_{on_min}			1.1		μs
Maximum On Time	T_{on_max}		6	7	8	μs
Minimum Off Time	T_{off_min}			2		μs
Maximum Off Time	T_{off_max}		500	600	700	μs
Maximum Frequency	f_{max}		108	120	130	kHz
CS						
Internal Reference Voltage	V_{REF}		0.204	0.210	0.216	V
CS Sampling Clamp Voltage	V_{CS_LMT}		1.1	1.2	1.3	V
CS Leading Edge Blanking Time	T_{LEB_CS}			350		ns
Switch off Delay Time	T_{DELAY_OFF}			200		ns
OVP						
OVP Voltage With Resistor	V_{OVP_RES}	R_{OVP} = 510 kohm	60			V
OVP Voltage With No Connection	V_{OVP_OPEN}		105			V
OVP Voltage With GND Short	V_{OVP_SC}		120			V
OVP Voltage With Resistor	V_{OVP_RES}	R_{OVP} = 120 kohm	160			V
MOSFET						
Drain-Source Breakdown Voltage	BV_{DSS_2302D}		700			V
	BV_{DSS_2302E}		650			
	BV_{DSS_2302E}		650			
Drain-Source On Resistance	$R_{DS\_ON\_2302D}$			4.5		ohm
	$R_{DS\_ON\_2302E}$			3.7		
	$R_{DS\_ON\_2302F}$			2.7		
Thermal Regulation						
Thermal Regulation Temperature	T_{OTR_TH}			145		℃

Note6: The max and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis.

Application Suggestion

YT2302XHS7 is a high precision active PFC driver integrating 800V JFET and 650V power MOSFET, specially designed for non-isolated buck offline constant current LED lighting. Operating in critical conduction mode, the driver achieves high power factor, low THD and high efficiency.

Start Up And Supply

When AC line is applied, main bus voltage can be built, then the JFET of the IC supply the inner operation. When the voltage of HV reaches VCC_ON, PWM is enabled; If the voltage of HV drops below the VCC_UVLO, PWM is disabled and restart is necessary.

Principle of The Active Power Factor Correction (APFC)

Constant on time (T_{on}) control with boundary conduction mode (BCM) operation is the key principle to achieve active power factor correction, thereby high power factor and low THD can be expected.

The power inductor is charged during the fixed T_{on} of the MOSFET, i_L increase linearly to the peak (i_{pk}) from zero; when MOSFET tuned off, the freewheeling diode release the inductor current, i_L decrease linearly from i_{pk} to zero and next switching cycle is triggered.

Fig. 4 shows the Key waveforms of the CC controlled buck with APFC.

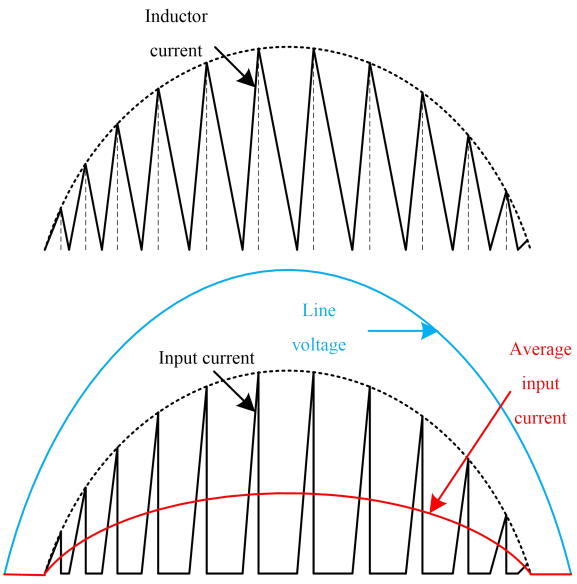


Fig. 4 Key waveforms of the CC controlled buck with APFC

Constant Current Control

In order to achieve high precision (±3%) output current (I_o) control, excellent line and load regulation, YT2302XHS7 operates in BCM and makes the real time sensing to the inductor current. I_o can be calculated with formula (1)

$$I_o = \frac{V_{ref}}{R_{cs}} \quad (1)$$

Where V_{ref} is the reference voltage， R_{cs} is the current sensing resistance.

Zero Current Detection (ZCD) and Valley Switching Technique

The zero crossing of the inductor current is detected for PWM turn-off signal, thereby the valley turn-on of the MOSFET and BCM operation of the inductor current can be achieved.

Maximum Off Time

Maximum off time (T_{off_max}) is set to avoid the condition that ZCD block missing the zero crossing event of the inductor current.

Minimum Off Time

Minimum off time (T_{off_min}) is set to limit the maximum switching frequency (f_{sw_max}), then the switching loss and EMC performance can be guaranteed. As shown in Fig. 5, PWM is triggered at the first valley after T_{off_min}.

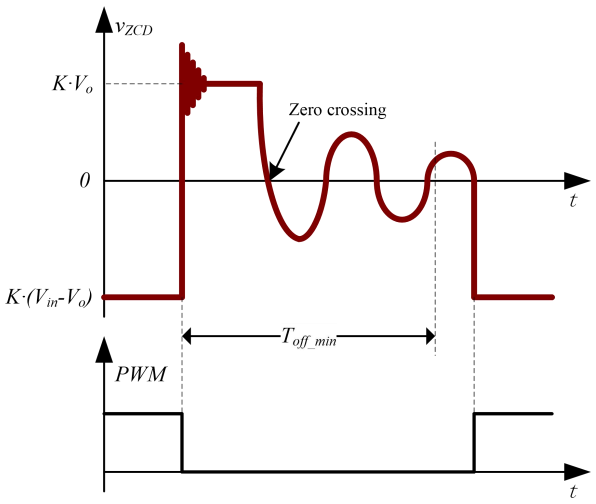


Fig. 5 Minimum off time

ZCD Blanking

Fig. 6 shows ZCD blanking time (T_{LEB_ZCD}) is set to avoid the fault trigger by the oscillation after the turn off.

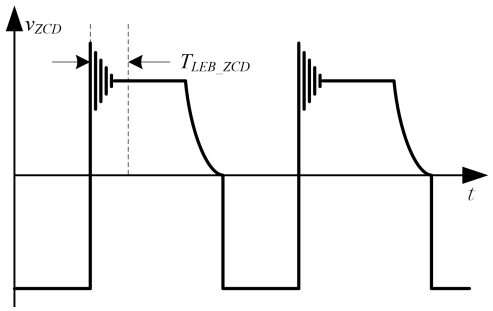


Fig. 6 ZCD blanking

CS Blanking

Fig. 7 shows CS blanking time (T_{LEB_CS}) is set to avoid the fault trigger by the oscillation after the turn on.

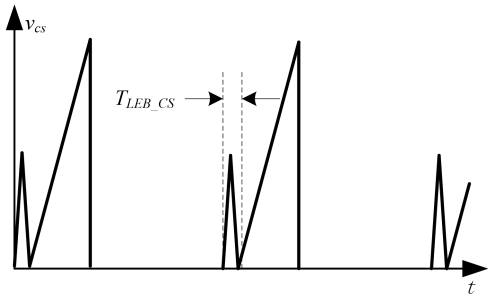


Fig. 7 CS blanking

Cycle by Cycle Current Limiting

When LED short or inductor saturation happens, CS pin voltage (V_{CS}) goes higher than regulation. However, CS voltage limit (V_{CS_LMT}) can help to stop PWM cycle by cycle to protect the MOSFET and the other power devices.

Over Temperature Regulation (OTR)

When the junction temperature goes higher than the threshold of the over temperature regulation (T_{OTR_TH}), chip will reduce the output current (I_o) by reducing the internal reference (V_{ref}). This is helpful to regulation the system temperature, guarantees the stability of both the driver and LED chip, and improves the reliability of the LED lighting system. Fig. 8 shows the principle of the over temperature regulation, where I_{o1} is the output current before OTR triggered; I_{o2} is the output current during OTR triggering and the junction temperature is T_{j2} for I_{o2}.

Over Voltage Protection

With different setting to OVP pin, customers can get

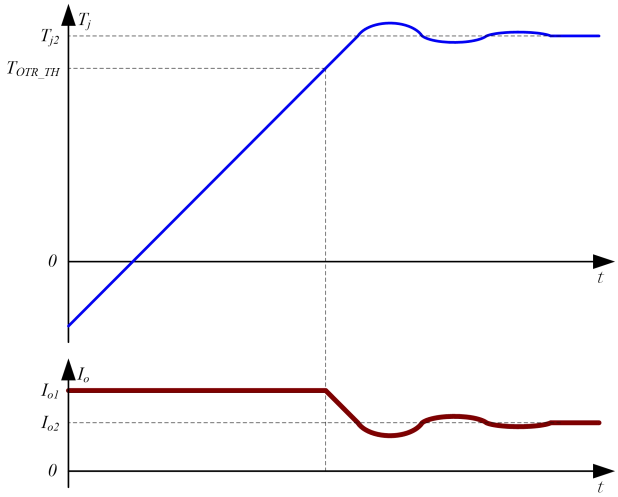


Fig. 8 Principle of the over temperature regulation

4 levels OVP for right application. Here we give the suggestion for maximum load voltage according to corresponding OVP lever with minimum 15kohm HV resistor.

OVP setting	OVP threshold	Max LED voltage
R_{OVP} = 510 *kohm*	60V	54V
Open to GND	105V	95V
Short to GND	120V	110V
R_{OVP} = 120 *kohm*	160V	150V

Current Dropping

Programmable current dropping at both low line (e.g. <180 Vac) and high line (e.g. > 350Vac) is designed to reduce the temperature of the components and system to improve the thermal and reliability performance.

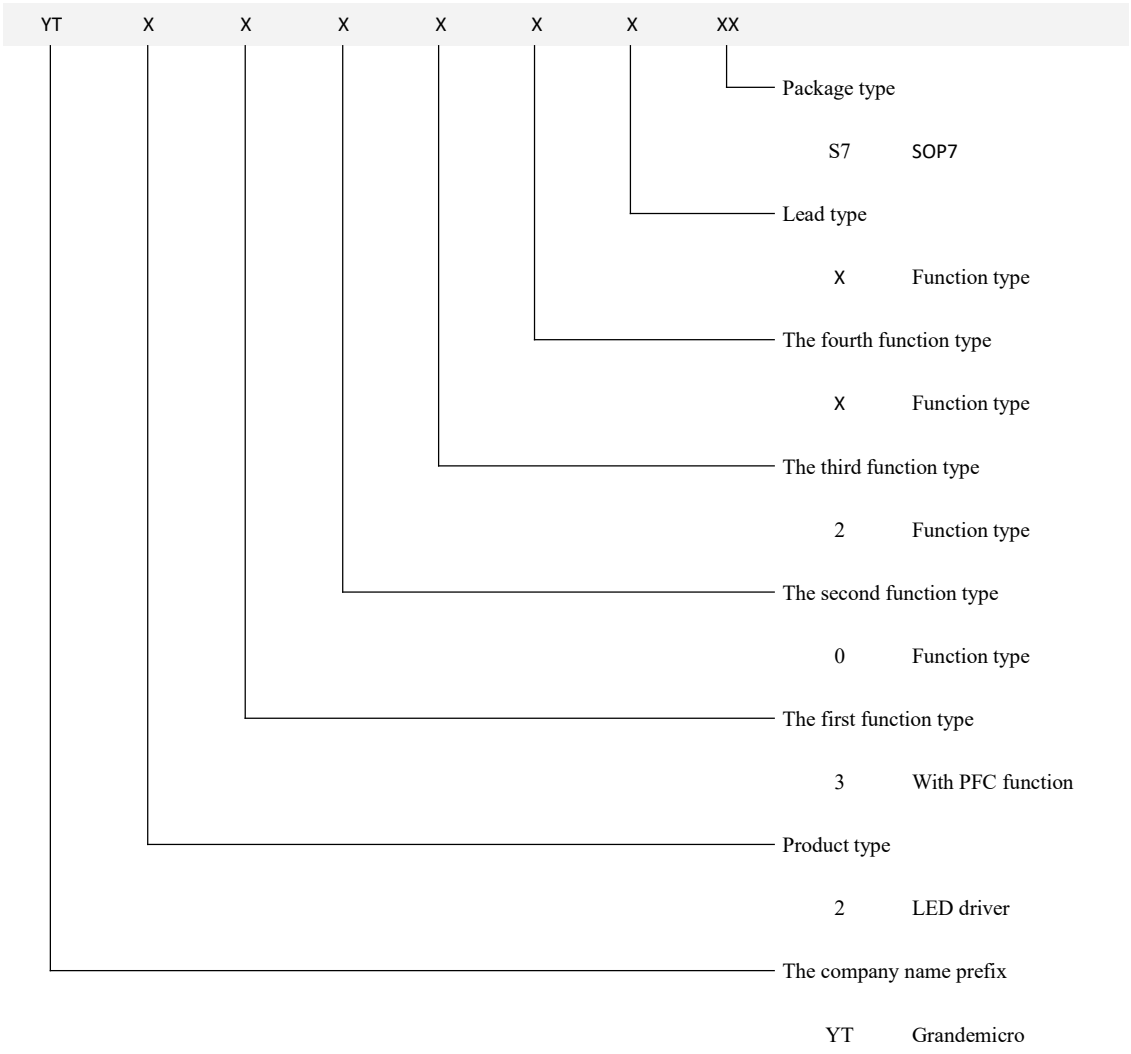
Restart after Protection

When PWM is stopped by any protection, chip increases the power dissipation to force VCC UVLO happen. Chip can only be restarted by VCC UVLO to remove the protection scheme.

PCB Design Guide

1. Current sensing resistor (R_{cs}) shall be placed very close to the chip, minimize the loop from CS pin to R_{cs} and GND pin.
2. Separate the power ground and the signal ground.
3. Minimize the loop from input capacitor (C_{in}) to MOSFET and the freewheeling diode to improve the system stability and EMC performance.

Marking Rule

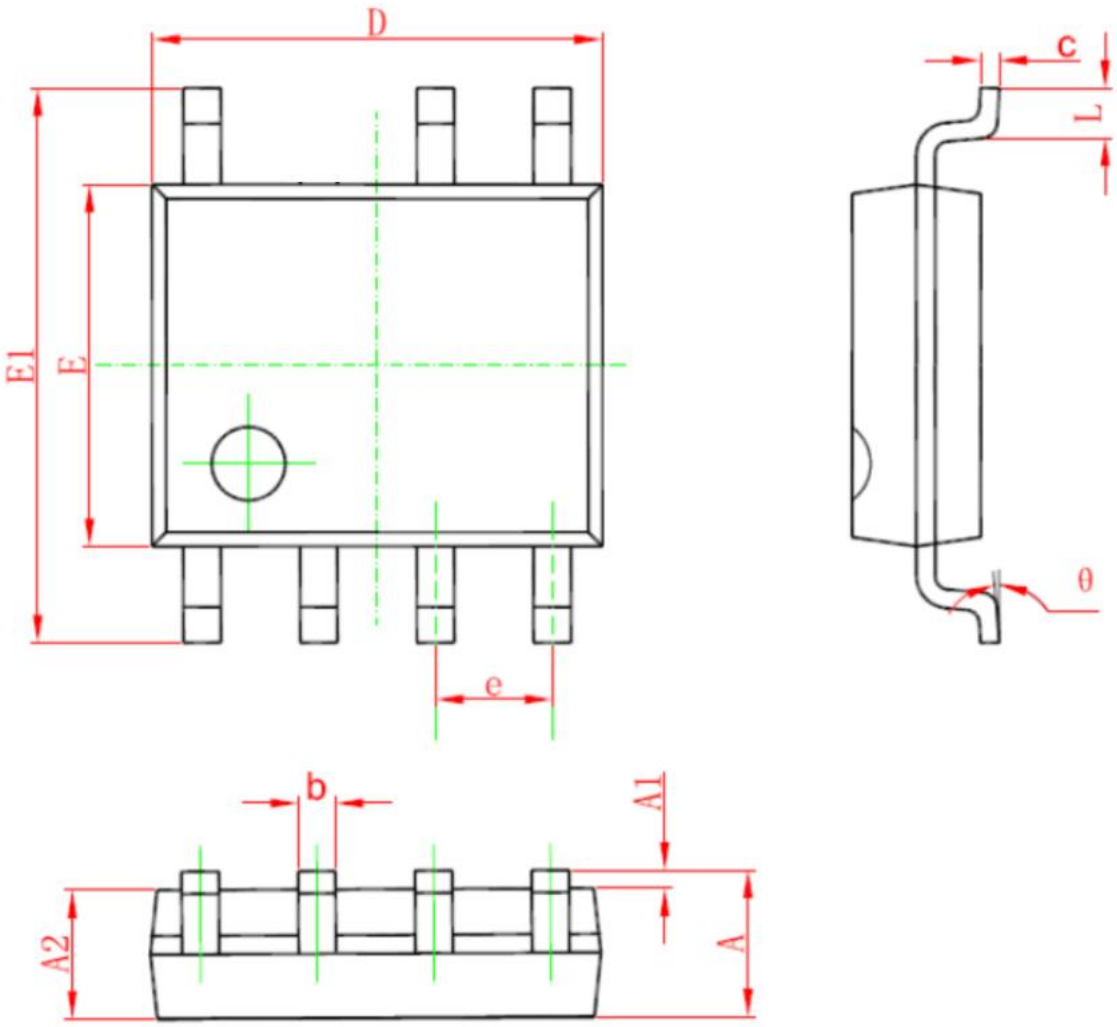


Naming Rule

●	Part No. Date Code Special Note
Part No.	YT2302BH, YT2302CH, YT2302DH, YT2302EH, YT2302FH
Date Code	P: Packing site; Y: Year; W: Week; S: Series; F: MOSFET.
Special Note	Use obvious mark like “H”, “L” to distinguish the key features like CS reference or OVP reference etc. if necessary.

Package

SOP7



Symbol	Size (mm)		Size (inch)	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270		0.050	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Version History

Version	Date	Description
A0	Jun. 2022	Draft
A1	Aug. 2022	Released
A2	June 2023	Update the MOS information
A3	Sep. 2023	Remove D version MOS, add G version MOS
A4	Nov. 2023	Change G version MOS to H version MOS due to the packaging issue.
A5	Dec. 2023	Update the CS reference to 210mV
A6	Jan. 2024	Update the Recommended Operation Conditions Remove H version MOS
A7	April 2025	Increase the D version MOSFET for kinds of applications